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(Modified)U.S. DEPARTMENT OF COMMERCE  
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251996US2

New Application

## LIST OF REFERENCES CITED BY APPLICANT

APPLICANT

Tomoaki SHINO

FILING DATE

Herewith

4/15/04

GROUP

2811

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
A.O.A.	AA	6,538,916	03/25/03	Takashi OHSAWA			
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION	
					YES	NO
A.O.A.	AO	2002-246571	08/30/02	Japan (with English Abstract and Corresponding U.S. Patent 6,538,916)		x
	AP					
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

A.O.A.	AW	Takashi OHSAWA, et al., "Memory Design Using a One-Transistor Gain Cell on SOI", IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. 37, No. 11, November 2002, pgs. 1510-1522				
	AX					
	AY					
	AZ					

☐ Additional References sheet(s) attached

Examiner

A.O.A.

Date Considered

1 July 05

\*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

CLASS  
2811  
CLASS